AMENDMENTS TO CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A deep trench structure of semiconductor device, said semiconductor device having a plurality of active areas, said deep trench structure having a deep trench communicating with only two different active areas which are respectively connected to two adjacent bit lines, so as to measure a leakage current between said two different active areas.

2. (Previously Presented) The structure as claimed in Claim 1, wherein the cross section of said deep trench communicates with said two different active areas.

3. (Canceled)

4. (Currently Amended) A semiconductor memory device comprising:

a plurality of bit lines;

a plurality of gates intersecting with said bit lines;

a plurality of active areas, each of which is connected to one of said bit lines;

a plurality of deep trenches, at least one of which communicates with only two different active areas which are respectively connected with two adjacent two of said bit lines, so as to measure a leakage current between said two different active areas.

5. (Previously Presented) The device as claimed in Claim 4, wherein the cross section of said deep trench communicates with said two different active areas.

6. (Canceled)